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Design of Low Power FFT Processor for OFDM Wireless Communication Systems

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Abstract— ***The demand for high-speed mobile wireless communications is rapidly growing. OFDM technology promises to be a key technique for achieving the high data capacity and spectral efficiency requirements for wireless communication systems of the near future. Fast Fourier transform (FFT) processing is one of the key procedures in popular orthogonal frequency division multiplexing (OFDM) communication systems. Structured pipeline architectures, low power consumption, high speed and reduced chip area are the main concerns in this VLSI implementation. In this paper, the efficient implementation of FFT processor for OFDM applications is presented. This processor can be used in various OFDM-based communication systems, such as Worldwide Interoperability for Microwave access (Wi-Max), digital audio broadcasting (DAB), digital video broadcasting-terrestrial (DVB-T). The three processing elements (PE's), delay-line (DL) buffers are used for computing FFT. Thus we consume low power, low hardware cost high efficiency and reduced chip size.***

Keywords— FFT, PE, Twiddle Factor, OFDM, Modified Booth Multiplier,SDF,Radix-2&4.

I.INTRODUCTION

The Fast Fourier Transform (FFT) are essential in the field of digital signal processing (DSP), widely used in communication systems , especially in orthogonal frequency division multiplexing (OFDM) systems, wireless-LAN, ADSL, VDSL systems and Wi-MAX. Apart from the applications, the system demands high speed of operation, low power consumption, reduced truncation error and reduced chip size.

By considering these facts, we proposed the ROM-less processor with single path delay feedback (SDF) pipeline architecture and modified booth width multiplier. The SDF pipelined architecture is used for the high- throughput in FFT processor.

There are three types of pipeline structures; they are single-path delay feedback (SDF), single-path delay commutator (SDC) and multi-path delay commutator. The advantages of single-path delay feedback (SDF). This SDF architecture is very simple to implement the different length FFT. The required registers in SDF architecture is less than MDC and SDC architectures. The control unit of SDF architecture is easier. We implement the processor in SDF architecture with radix-4 algorithm.

There are various algorithms to implement FFT, such as radix-2, radix-4 and split-radix with arbitrary sizes. Radix-2 algorithm is the simplest one, but its calculation of addition and multiplication is more than radix-4's. Though being more efficient than radix-2, radix-4 only can process 4n point FFT.

The radix-4 FFT equation essentially combines two stages of a radix-2 FFT into one, so that half as many stages are required. Since the radix-4 FFT requires fewer stages and butterflies than the radix 2 FFT, the computations of FFT can be further improved. In order to speed up the FFT computation we increase the radix, for reducing the chip size we use ROM-less architecture and for further low power consumption we implement the reconfigurable complex multiplier and delay line buffers , error compensation is carried out using fixed width modified booth multiplier.

Several error compensation methods have been proposed here, the fixed width modified booth multipliers achieve better error performance in terms of absolute error and mean square error. Using radix-4 algorithm, we propose a 64-point FFT processor with ROM less architecture.

II. EXISTING SYSTEM

In last three decades, various FFT architectures such as single-memory architecture, dual memory architecture, pipelined architecture, array architecture and cache memory architecture have been proposed.

In order to improve the power reduction, we propose a radix-4 64-point pipeline FFT processor. In order to speed up the FFT computations, more advanced solutions have been proposed using an increase of the radix. The radix-4 FFT

algorithm is most popular and has the potential to satisfy the current need.

The radix-4 FFT equation essentially combines two stages of a radix-2 FFT into one, so that half as many stages are required. To calculate 16-point FFT, the radix-2 takes log216=4 stages but the radix-4 takes only log416=2 stages. A 16-point, radix-4 decimation-in-frequency FFT algorithm is shown in Figure 1.

Its input is in normal order and its output is in digit-reversed order. It has exactly the same computational complexity as the decimation-in-time radix-4 FFT algorithm. When the number of data points N in the DFT is a power of 4, then is more efficient computationally to employ a radix-4 algorithm instead of radix-2 algorithm.

A radix-4 decimation in-time FFT algorithm is obtained by splitting the N point input sequence x(n)into four sub sequences x(4n), x(4n +1), x(4n + 2) and x(4n + 3).

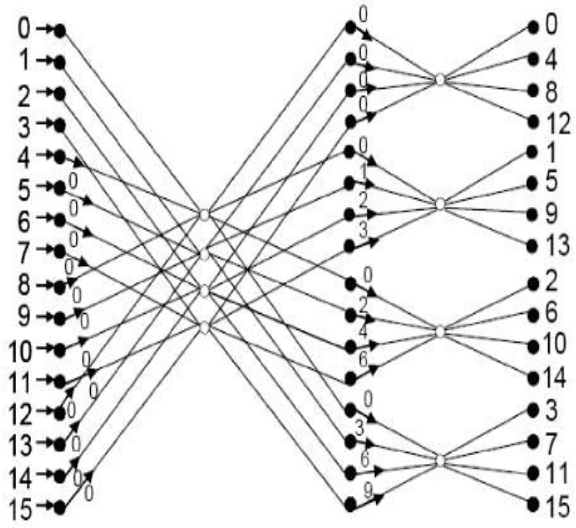

Figure.1 Flow graph of existing 16-point radix-4 FFT algorithm.

The radix-4 decimation in frequency butterfly is constructed by merging 4-point DFT with associated coefficients between DFT stages. The four outputs of the radix-4 butterfly namely X(4n), X(4n+1), X(4N+2) and X(4N+3) are expressed in terms of its inputs x(n), x(n)+N/4 , x(n)+N/2 and x(n)+3N/4.

III. PROPOSED SYSTEM

In this paper, low power techniques are employed for power consumption using reconfigurable complex multiplier. Using radix-4 algorithm, increase the computational speed, further reduce the chip area by three different processing elements (PE's) were proposed in this radix-4 64-point FFT processor.

Our proposed architecture uses a low complexity reconfigurable complex multiplier instead of ROM tables to generate twiddle factors and fixed width modified booth multiplier to reduce the truncation error.

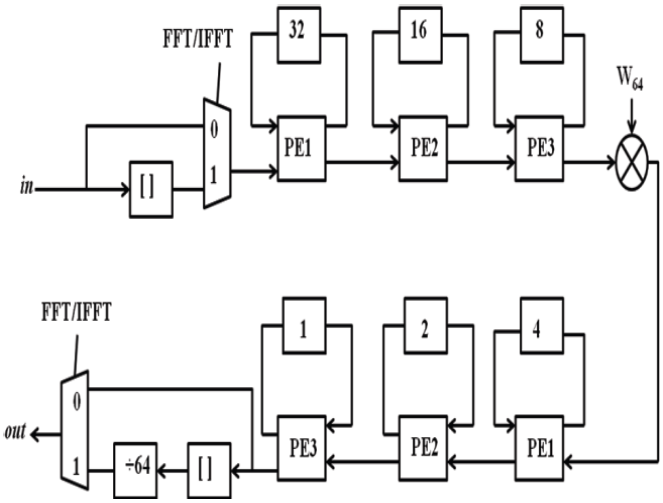

Figure.2 Proposed radix-4 64-point pipeline FFT processor

This proposed architecture consists of three different types of processing elements (PEs), reconfigurable constant complex multiplier, delay line buffers (as shown by a rectangle with a number inside).

Here, the conjugate operation is easy to implement, where we have to generate the 2's complement of the imaginary part of a complex value. This new multiplication structure becomes the key component in reducing the chip area and power consumption. Based on the radix-4 FFT algorithm, the three types of processing elements (PE3, PE2, PE1) proposed in our design. Illustrated in fig.3, fig.4, and fig.5 respectively.

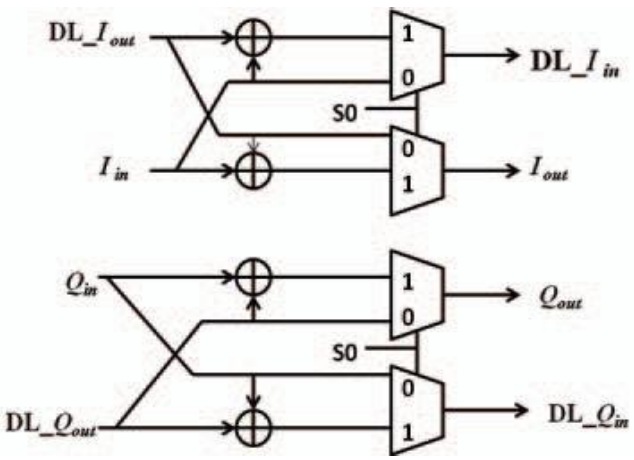

Figure.3 Circuit diagram of our proposed PE3 stage.

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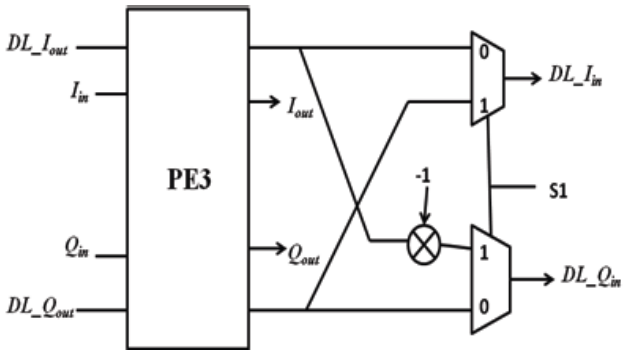

Figure.4 Circuit diagram of our proposed PE2 stage.

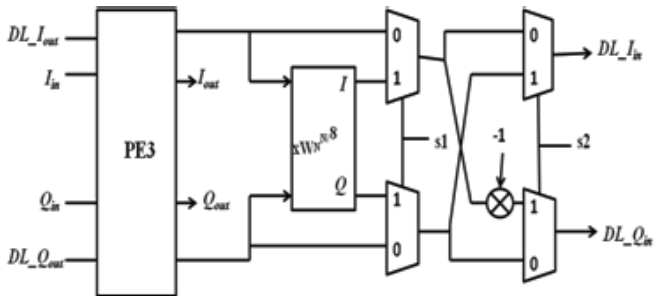

Figure.5 Circuit diagram of our proposed PE1 stage.

The PE3 stage is used to implement the radix-4 Butterfly structure, and serves as sub-modules of the PE2 and PE1 stages. In the PE2 stage, the calculation of multiplication by –j or 1 uses the outcome of the PE3 module. Note that a multiplication by -1 is practically to take the 2's complement of the input value. The PE1 stage is responsible for computing the multiplications by –j, WN N/8, and WN 3N/8, respectively. Since WN 3N/8= -jWN 3N/8, it can be done with a multiplication by, WN N/8 first and then a multiplication by –j. Hence, our designed hardware utilizes this kind of cascaded calculation and multiplexers to realize all the calculations in the PE1 stage. The realization of multiplication by, WN N/8 using radix-4 butterfly structure with its both outputs commonly multiplied by 1/√2, is shown in fig.6

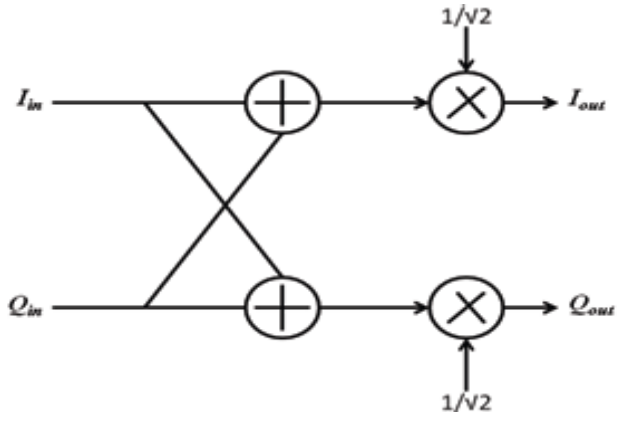

Figure.6 Circuit diagram of the multiplication by WN N/8

Here the multiplication operation of modified booth multipliers, the multiplication operation of A=an-1an-2....a0 (multiplicand) and B= bn-1bn-2....b0 (multiplier) can be expressed as follows:

$$A = -a_{n-1}2^{n-1} + \sum_{i=0}^{n-2} a_i 2^i, \quad B = -b_{n-1}2^{n-1} + \sum_{i=0}^{n-2} b_i 2^i.$$

$$B = \sum_{i=0}^{n/2-1} M_i 2^{2i} = \sum_{i=0}^{n/2-1} (-2b_{2i+1} + b_{2i} + b_{2i-1})2^{2i}$$

The modified booth encoder and partial product generation circuit shown in fig.7

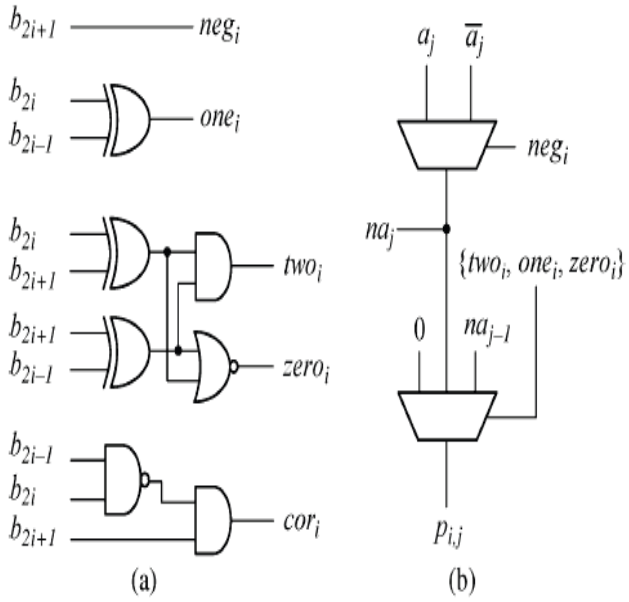

Figure.7 (a) modified booth encoder. (b) Partial product generation circuit.

Here the partial product matrix of booth multiplication was slightly modified and effective error compensation was derived. The output quality in terms of peak signal to noise ratio (PSNR) for different fixed-width booth multipliers are used in different applications.

IV.CONCLUSION

A low power pipelined 64-point FFT processor for OFDM applications has been described in this paper. This designed hardware requires about 33.6k gates, and has a working frequency up to 80 MHz synthesized by using 0.18μm CMOS technology. Since this design requires low-cost and consumes low power, as well as reduced SQNR and highly efficient. Hence it can be applied as a powerful FFT processor in wireless communication systems in future.

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